

What is claimed is:

1. A semiconductor device comprising:

a semiconductor substrate;

5 source and drain electrodes, which are formed on the semiconductor substrate to make ohmic contact with the semiconductor substrate;

a T-shaped gate electrode, which is formed between the source and drain electrodes on the semiconductor substrate; and

10 an insulating layer including a silica aerogel layer, the silica aerogel layer being interposed between the gate electrode and the source and drain electrodes.

2. The semiconductor device of claim 1, wherein the insulating layer is formed of a composite layer of the silicon nitride layer and the silica aerogel layer.

15 3. The semiconductor device of claim 2, wherein the silica aerogel layer has a thickness greater than the thickness of the silicon nitride layer.

4. The semiconductor device of claim 2, wherein the silicon nitride layer has a thickness of 100-1000 Å.

20 5. The semiconductor device of claim 1, wherein the silica aerogel layer has a thickness of 1000-3000 Å.

6. A method of manufacturing a semiconductor device, the method comprising:

25 forming an insulating layer pattern on a semiconductor substrate, the insulating layer pattern being formed of a composite layer of a first insulating layer and a silica aerogel layer and defining a first opening through which a first portion of the semiconductor substrate is exposed;

30 forming source and drain electrodes on the semiconductor substrate exposed through the first opening;

forming a second insulating layer for covering the source and drain electrodes and the insulating layer pattern;

patterning the second insulating layer and the insulating layer pattern to form a second opening through which a second portion of the semiconductor substrate is exposed, between the source and drain electrodes; and

forming a T-shaped gate electrode on the semiconductor substrate exposed through the second opening.

7. The method of claim 6, wherein the second insulating layer is formed of silica aerogel.

8. The method of claim 6, wherein the forming the insulating layer pattern includes:

forming the first insulating layer on the semiconductor substrate; and

forming the silica aerogel layer on the first insulating layer.

9. The method of claim 6, further comprising etching the semiconductor substrate exposed through the second opening to form a recess region in the semiconductor substrate, wherein the gate electrode is formed in the recess region.

10. The method of claim 6, wherein the first insulating layer is a silicon nitride layer.

11. A method of manufacturing a semiconductor device, the method comprising:

forming source and drain electrodes on a semiconductor substrate;

forming a first insulating layer for covering the source and drain electrodes and a top surface of the semiconductor substrate;

forming a silica aerogel layer on the first insulating layer;

patterning the silica aerogel layer and the first insulating layer to expose a first portion of the semiconductor substrate; and

forming a T-shaped gate electrode on the first exposed portion.

12. The method of claim 11, wherein the first insulating layer is a silicon nitride layer.